



## 2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL, VLP

### FEATURES

- 240-pin, dual in-line very low profile (VLP) memory module
- Fast data transfer rates: PC2-6400\*, PC2-5300\*, PC2-4300 and PC2-3200
- Utilizes 800, 667, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V$
- $V_{CCSPD} = +1.7V$  to  $+3.6V$
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# additive latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- ECC error detection and correction
- Dual Rank
- RoHS compliant
- Package option
  - 240 Pin VLP: 18.29mm (0.720") TYP

### DESCRIPTION

The W3HG2128M72ACER is a 2x128Mx72 Double Data Rate DDR2 SDRAM high density module based on DDR2 SDRAM components. This memory module consists of eighteen stacks of 256Mx4 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

\* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option
- Parity function

### OPERATING FREQUENCIES

	PC2-3200	PC2-4300	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-tRCD-tRP	3-3-3	4-4-4	5-5-5	6-6-6

\* Consult factory for availability



**PIN CONFIGURATION**

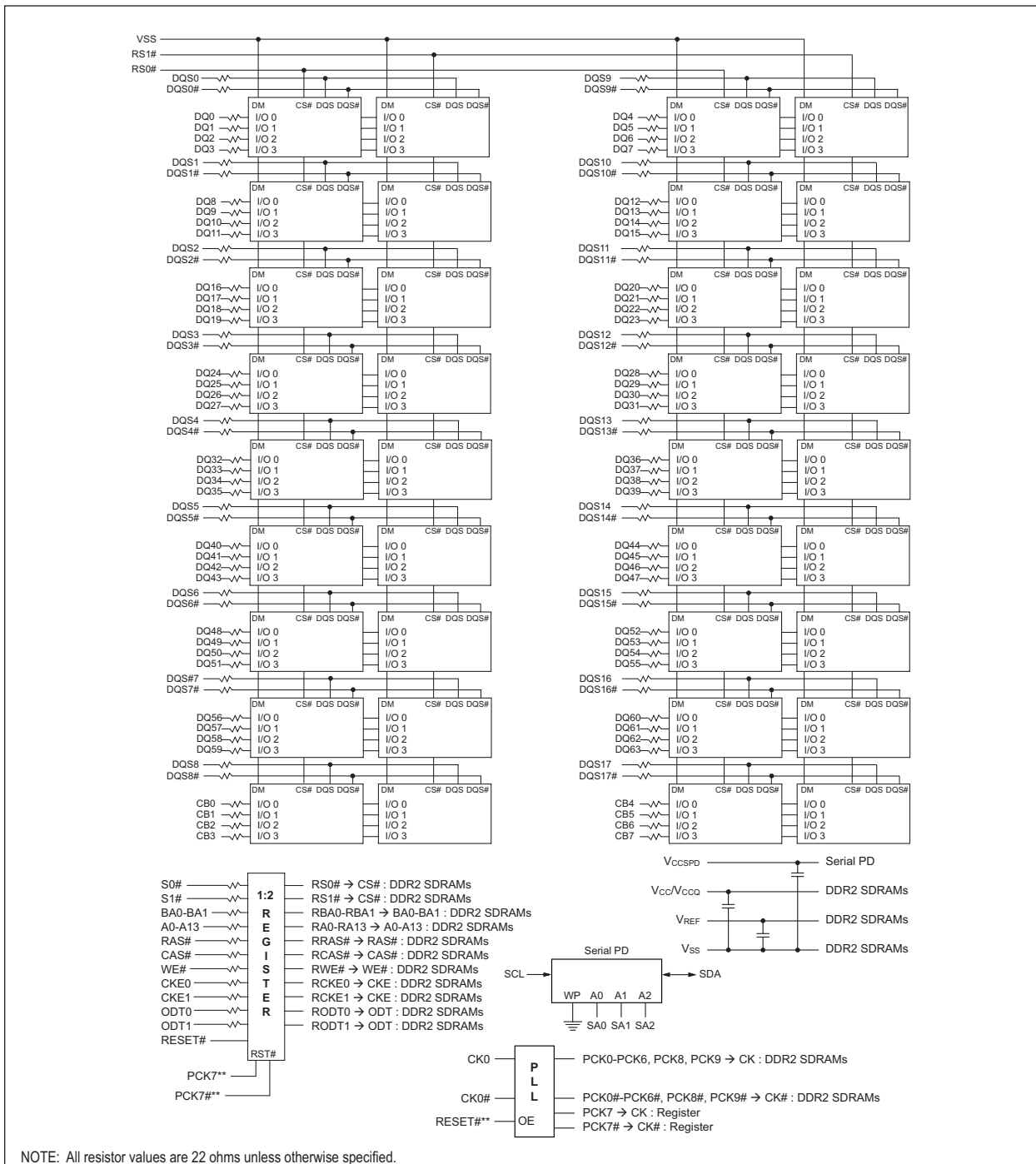
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V <sub>REF</sub>	61	A4	121	V <sub>SS</sub>	181	V <sub>CCQ</sub>
2	V <sub>SS</sub>	62	V <sub>CCQ</sub>	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	V <sub>CC</sub>	124	V <sub>SS</sub>	184	V <sub>CC</sub>
5	V <sub>SS</sub>	65	V <sub>SS</sub>	125	DQS9	185	CK0
6	DQS0#	66	V <sub>SS</sub>	126	DQS9#	186	CK0#
7	DQS0	67	V <sub>CC</sub>	127	V <sub>SS</sub>	187	V <sub>CC</sub>
8	V <sub>SS</sub>	68	NC/PAR_IN	128	DQ6	188	A0
9	DQ2	69	V <sub>CC</sub>	129	DQ7	189	V <sub>CC</sub>
10	DQ3	70	A10/AP	130	V <sub>SS</sub>	190	BA1
11	V <sub>SS</sub>	71	BA0	131	DQ12	191	V <sub>CCQ</sub>
12	DQ8	72	V <sub>CCQ</sub>	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	V <sub>SS</sub>	193	S0#
14	V <sub>SS</sub>	74	CAS#	134	DQS10	194	V <sub>CCQ</sub>
15	DQS1#	75	V <sub>CCQ</sub>	135	DQS10#	195	ODT0
16	DQS1	76	S1#	136	V <sub>SS</sub>	196	A13
17	V <sub>SS</sub>	77	ODT1	137	NC	197	V <sub>CC</sub>
18	RESET#	78	V <sub>CCQ</sub>	138	NC	198	V <sub>SS</sub>
19	NC	79	V <sub>SS</sub>	139	V <sub>SS</sub>	199	DQ36
20	V <sub>SS</sub>	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	V <sub>SS</sub>
22	DQ11	82	V <sub>SS</sub>	142	V <sub>SS</sub>	202	DQS13
23	V <sub>SS</sub>	83	DQS4#	143	DQ20	203	NC/DQS13#
24	DQ16	84	DQS4	144	DQ21	204	V <sub>SS</sub>
25	DQ17	85	V <sub>SS</sub>	145	V <sub>SS</sub>	205	DQ38
26	V <sub>SS</sub>	86	DQ34	146	DQS11	206	DQ39
27	DQS2#	87	DQ35	147	DQS11#	207	V <sub>SS</sub>
28	DQS2	88	V <sub>SS</sub>	148	V <sub>SS</sub>	208	DQ44
29	V <sub>SS</sub>	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	V <sub>SS</sub>
31	DQ19	91	V <sub>SS</sub>	151	V <sub>SS</sub>	211	DQS14
32	V <sub>SS</sub>	92	DQS5#	152	DQ28	212	NC/DQS14#
33	DQ24	93	DQS5	153	DQ29	213	V <sub>SS</sub>
34	DQ25	94	V <sub>SS</sub>	154	V <sub>SS</sub>	214	DQ46
35	V <sub>SS</sub>	95	DQ42	155	DQS12	215	DQ47
36	DQS3#	96	DQ43	156	DQS12#	216	V <sub>SS</sub>
37	DQS3	97	V <sub>SS</sub>	157	V <sub>SS</sub>	217	DQ52
38	V <sub>SS</sub>	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	V <sub>SS</sub>
40	DQ27	100	V <sub>SS</sub>	160	V <sub>SS</sub>	220	NC
41	V <sub>SS</sub>	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V <sub>SS</sub>
43	CB1	103	V <sub>SS</sub>	163	V <sub>SS</sub>	223	DQS15
44	V <sub>SS</sub>	104	DQS6#	164	DQS17	224	NC/DQS15#
45	DQS8#	105	DQS6	165	DQS17#	225	V <sub>SS</sub>
46	DQS8	106	V <sub>SS</sub>	166	V <sub>SS</sub>	226	DQ54
47	V <sub>SS</sub>	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	V <sub>SS</sub>
49	CB3	109	V <sub>SS</sub>	169	V <sub>SS</sub>	229	DQ60
50	V <sub>SS</sub>	110	DQ56	170	V <sub>CCQ</sub>	230	DQ61
51	V <sub>CCQ</sub>	111	DQ57	171	CKE1	231	V <sub>SS</sub>
52	CKE0	112	V <sub>SS</sub>	172	V <sub>CC</sub>	232	DQS16
53	V <sub>CC</sub>	113	DQS7#	173	NC	233	NC/DQS16#
54	NC	114	DQS7	174	NC	234	V <sub>SS</sub>
55	NC/ERR_OUT	115	V <sub>SS</sub>	175	V <sub>CCQ</sub>	235	DQ62
56	V <sub>CCQ</sub>	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	V <sub>SS</sub>
58	A7	118	V <sub>SS</sub>	178	V <sub>CC</sub>	238	V <sub>CC</sub> SPD
59	V <sub>CC</sub>	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

**PIN NAMES**

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes complement
DM0-DM8	Data Masks
DQS9#-DQS17#	Data Strobe Negative
DQS9-DQS17	Data Strobe
ODT0, ODT1	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0, CKE1	Clock Enables
S0#, S1#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect (SPD) Clock Input
V <sub>CC</sub>	Core Power (1.8V)
V <sub>CCQ</sub>	I/O Power (1.8V)
V <sub>SS</sub>	Ground
V <sub>REF</sub>	Power Supply for Reference
V <sub>CC</sub> SPD	SPD Power
NC	Spare pins, No connect



**FUNCTIONAL BLOCK DIAGRAM**





**RECOMMENDED DC OPERATING CONDITIONS**

All Voltages Referenced to Vss

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	Vcc	1.7	1.8	1.9	V	4
Supply Voltage for DLL	Vccl	1.7	1.8	1.9	V	4
Supply Voltage for Output	Vccq	1.7	1.8	1.9	V	4
Input Reference Voltage	VREF	0.49*Vccq	0.50*Vccq	0.51*Vccq	V	1, 2
Termination Voltage	VTT	VREF-0.04	VREF	VREF+0.04	V	3

There is no specific device Vcc supply voltage requirement for SSTL-1.8 compliance. However under all conditions Vccq must be less than or equal to Vcc.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x Vccq of the transmitting device and VREF is expected to track variations in Vccq.
2. Peak to peak AC noise on VREF may not exceed ±2% VREF(DC).
3. VTT of transmitting device must track VREF of receiving device.
4. Vcc, Vccq and Vccl are tied together on this module.

**ABSOLUTE MAXIMUM RATINGS**

SSTL\_1.8V

Symbol	Parameter	Rating	Units	Notes
Vcc	Voltage on Vcc pin relative to Vss	- 1.0 V - 2.3 V	V	5
Vccq	Voltage on Vccq pin relative to Vss	- 0.5 V - 2.3 V	V	5
Vccl	Voltage on Vccl pin relative to Vss	- 0.5 V - 2.3 V	V	5
VIN, VOUT	Voltage on any pin relative to Vss	- 0.5 V - 2.3 V	V	5
TSTG	Storage Temperature	-55 to +100	C	5, 6

5. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
6. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

**CAPACITANCE**

TA = 25°C, f = VREF = Gnd, f = 100MHz, Vcc = Vccq = 1.8V

Parameter	Symbol	Max	Units
Input Capacitance: CK, CK#	Cck	5.6	pF
Input Capacitance: KE, CS#	Cl1	12.4	pF
Input Capacitance: Addr. RAS#, CAS#, WE#, ODT	Cl2	12.4	pF
Input/Output Capacitance: DQ, DQS, DM, DQS#, CB	Cl0	15.6	pF



**DDR2 Icc SPECIFICATIONS AND CONDITIONS**

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions	806	665	534	403	Units	
I <sub>CC0</sub>	Operating one bank active-precharge current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,720	1,530	1,530	mA	
I <sub>CC1</sub>	Operating one bank active-read-precharge current; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>CC4W</sub>	TBD	1,980	1,800	1,710	mA	
I <sub>CC2P</sub>	Precharge power-down current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	180	180	180	mA	
I <sub>CC2Q</sub>	Precharge quiet standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	1,800	1,440	1,260	mA	
I <sub>CC2N</sub>	Precharge standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,980	1,620	1,440	mA	
I <sub>CC3P</sub>	Active power-down current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	1,260	1,080	900	mA
		Slow PDN Exit MRS(12) = 1	TBD	360	360	360	mA
I <sub>CC3N</sub>	Active standby current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	2,340	1,980	1,620	mA	
I <sub>CC4W</sub>	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	2,880	2,430	2,070	mA	
I <sub>CC4R</sub>	Operating burst read current; All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>CC4W</sub>	TBD	3,240	2,700	2,160	mA	
I <sub>CC5B</sub>	Burst auto refresh current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); Refresh command at every t <sub>REFC</sub> (I <sub>CC</sub> ) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	7,560	7,200	6,840	mA	
I <sub>CC6</sub>	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	TBD	180	180	180	mA	
I <sub>CC7</sub>	Operating bank interleave read current; All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = t <sub>RCD</sub> (I <sub>CC</sub> )-1*t <sub>CK</sub> (I <sub>CC</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RRD</sub> = t <sub>RRD</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = 1*t <sub>CK</sub> (I <sub>CC</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I <sub>CC4R</sub> ; Refer to the following page for detailed timing conditions	TBD	5,130	4,770	4,230	mA	

NOTE: Icc specs are based on MICRON components. Other DRAM manufacturers parameters may be different.



**AC TIMING PARAMETERS**

0°C ≤ T<sub>CASE</sub> < +85°C; V<sub>CCQ</sub> = +1.8V ± 0.1V, V<sub>CC</sub> = +1.8V ± 0.1V

AC CHARACTERISTICS			806		667		534		403				
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	Notes	
Clock	Clock cycle time	CL = 6	t <sub>CK(6)</sub>	TBD	TBD						ps	16, 24	
		CL = 5	t <sub>CK(5)</sub>	TBD	TBD	3,000	8,000				ps	16, 24	
		CL = 4	t <sub>CK(4)</sub>	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps	16, 24
		CL = 3	t <sub>CK(3)</sub>	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps	16, 24
	CK high-level width	t <sub>CH</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	tck	18	
	CK low-level width	t <sub>CL</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	tck	18	
	Half clock period	t <sub>HP</sub>	TBD	TBD	MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		ps	19	
Data	DQ output access time from CK/CK#	t <sub>AC</sub>	TBD	TBD	-450	+450	-500	+500	-600	+600	ps		
	Data-out high-impedance window from CK/CK#	t <sub>HZ</sub>	TBD	TBD		t <sub>AC</sub> (MAX)		t <sub>AC</sub> MAX		t <sub>AC</sub> MAX	ps	8, 9	
	Data-out low-impedance window from CK/CK#	t <sub>LZ</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	ps	8, 10	
	DQ and DM input setup time relative to DQS	t <sub>DSa</sub>	TBD	TBD	300		350		400		ps	7, 15, 21	
	DQ and DM input hold time relative to DQS	t <sub>DHa</sub>	TBD	TBD	300		350		400		ps	7, 15, 21	
	DQ and DM input setup time relative to DQS	t <sub>DSb</sub>	TBD	TBD	100		100		150		tck	7, 15, 21	
	DQ and DM input hold time relative to DQS	t <sub>DHb</sub>	TBD	TBD	175		225		275		ps	7, 15, 21	
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access relative to DQS	t <sub>DIPW</sub>	TBD	TBD	0.35		0.35		0.35		ps		
	Data hold skew factor	t <sub>QHS</sub>	TBD	TBD		340		400		450			
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t <sub>QH</sub>	TBD	TBD	t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>			15, 17	
	Data valid output window (DVW)	t <sub>DVW</sub>	TBD	TBD	t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>			15, 17	
Data Strobe	DQS input high pulse width	t <sub>DQSH</sub>	TBD	TBD	0.35		0.35		0.35		tck		
	DQS input low pulse width	t <sub>DQSL</sub>	TBD	TBD	0.35		0.35		0.35		tck		
	DQS output access time from CK/CK#	t <sub>DQSCK</sub>	TBD	TBD	-400	+400	-450	+450	-500	+500	ps		
	DQS falling edge to CK rising- setup time	t <sub>DSS</sub>	TBD	TBD	0.2		0.2		0.2		tck		
	DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	TBD	TBD	0.2		0.2		0.2		tck		
	DQS-DQ skew, DQS to last DQ valid, per group, per access	t <sub>DQSQ</sub>	TBD	TBD		240		300		350	ps	15, 17	
	DQS read preamble	t <sub>RPRE</sub>	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	tck	35	

NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.



**AC TIMING PARAMETERS (Continued)**

0°C ≤ T<sub>case</sub> < +85°C; V<sub>CCQ</sub> = + 1.8V ± 0.1V, V<sub>CC</sub> = +1.8V ± 0.1V

	AC CHARACTERISTICS		806		665		534		403		UNIT	Notes
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Data Strobe	DQS read preamble	t <sub>RPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	35
	DQS write preamble setup time	t <sub>WPRES</sub>	TBD	TBD	0		0		0		ps	12, 13, 36
	DQS write preamble	t <sub>WPRE</sub>	TBD	TBD	0.35		0.25		0.25		t <sub>CK</sub>	
	DQS write postamble	t <sub>WPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	11
	Write command to first DQS latching transition	t <sub>DQSS</sub>	TBD	TBD	WL-0.25		WL-0.25		WL-0.25		t <sub>CK</sub>	
Command and Address	Address and control input pulse width for each input	t <sub>IPW</sub>	TBD	TBD	0.6		0.6		0.6		t <sub>CK</sub>	
	Address and control input setup time	t <sub>ISa</sub>	TBD	TBD	400		500		600		ps	6, 21
	Address and control input hold time	t <sub>IHa</sub>	TBD	TBD	400		500		600		ps	6, 21
	Address and control input setup time	t <sub>ISb</sub>	TBD	TBD	200		250		350		ps	6, 21
	Address and control input hold time	t <sub>IHb</sub>	TBD	TBD	275		375		475		ps	6, 21
	CAS# to CAS# command delay	t <sub>CCD</sub>	TBD	TBD	2		2		2		t <sub>CK</sub>	
	Active to Active (same bank) command	t <sub>RC</sub>	TBD	TBD	55		55		55		ns	33
	Active bank a to Active b bank command	t <sub>R RD</sub>	TBD	TBD	7.5		7.5		7.5		ns	27
	Active to Read or Write delay	t <sub>RC D</sub>	TBD	TBD	15		15		15		ns	
	Four Bank Activate period	t <sub>FAW</sub>	TBD	TBD	37.5		37.5		37.5		ns	30
	Active to precharge command	t <sub>RAS</sub>	TBD	TBD	40	70,000	40	70,000	40	70,000	ns	20, 33
	Internal Read to precharge command delay	t <sub>RTP</sub>	TBD	TBD	7.5		7.5		7.5		ns	23, 27
	Write recovery time	t <sub>WR</sub>	TBD	TBD	15		15		15		ns	27
	Auto precharge write recovery and precharge time	t <sub>DAL</sub>	TBD	TBD	t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		ns	22
	Interval Write to Read command delay	t <sub>WTR</sub>	TBD	TBD	10		7.5		10		ns	27
	Precharge command period	t <sub>RP</sub>	TBD	TBD	15		15		15		ns	31
	Precharge All command period	t <sub>RPA</sub>	TBD	TBD	t <sub>RP</sub> +t <sub>CK</sub>		t <sub>RP</sub> +t <sub>CK</sub>		t <sub>RP</sub> +t <sub>CK</sub>		ns	31
Load Mode command cycle time	t <sub>MRD</sub>	TBD	TBD	2		2		2		t <sub>CK</sub>		
CKE low to CK,CK# uncertainty	t <sub>DELAY</sub>	TBD	TBD	t <sub>IS</sub> +t <sub>CK</sub> +t <sub>IH</sub>		t <sub>IS</sub> +t <sub>CK</sub> +t <sub>IH</sub>		t <sub>IS</sub> +t <sub>CK</sub> +t <sub>IH</sub>		ns	28	

NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.



**AC TIMING PARAMETERS (Continued)**

0°C ≤ T<sub>CASE</sub> < +85°C; V<sub>CCQ</sub> = + 1.8V ± 0.1V, V<sub>CC</sub> = +1.8V ± 0.1V

	AC CHARACTERISTICS		806		665		534		403		UNIT	Notes
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Self Refresh	Refresh to Active or Refresh to Refresh command interval	t <sub>RFC</sub> (2GB)	TBD	TBD	105	70,000	105	70,000	105	70,000	ns	14
		t <sub>RFC</sub> (4GB)	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns	14
	Average periodic refresh interval	t <sub>REFI</sub>	TBD	TBD	200	7.8		7.8		7.8	µs	14
	Exit self refresh to non-read command	t <sub>XSNR</sub>	TBD	TBD	t <sub>RFC</sub> (MIN)+10		t <sub>RFC</sub> (MIN)+10		t <sub>RFC</sub> (MIN)+10		ns	
	Exit self refresh to read command	t <sub>XSRD</sub>	TBD	TBD	200		200		200		t <sub>CK</sub>	
	Exit self refresh timing reference	t <sub>ISXR</sub>	TBD	TBD	t <sub>IS</sub>		t <sub>IS</sub>		t <sub>IS</sub>		ps	6, 29
ODT	ODT turn-on delay	t <sub>AOND</sub>	TBD	TBD	2	2	2	2	2	2	t <sub>CK</sub>	
	ODT turn-on	t <sub>AON</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+700	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+1,000	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+1,000	ps	25
	ODT turn-off delay	t <sub>AOFD</sub>	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t <sub>CK</sub>	
	ODT turn-off	t <sub>AOF</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)+600	ps	26
	ODT turn-on (power-down mode)	t <sub>AONPD</sub>	TBD	TBD	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	ps	
	ODT turn-off (power-down mode)	t <sub>AOFFPD</sub>	TBD	TBD	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	t <sub>AC</sub> (MIN)+2,000	2x t <sub>CK</sub> + t <sub>AC</sub> (MAX)+1,000	t <sub>CK</sub>	
	ODT to power-down entry latency	t <sub>ANPD</sub>	TBD	TBD	3		3		3		t <sub>CK</sub>	
	ODT power-down exit latency	t <sub>AXPD</sub>	TBD	TBD	8		8		8		t <sub>CK</sub>	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t <sub>XARD</sub>	TBD	TBD	2		2		2		t <sub>CK</sub>	
	Exit active power-down to READ command, MR[bit12=1]	t <sub>XARDS</sub>	TBD	TBD	7-AL		6-AL		6-AL		t <sub>CK</sub>	
	Exit precharge power-down to any non-READ command.	t <sub>XP</sub>	TBD	TBD	2		2		2		t <sub>CK</sub>	
	CKE minimum high/low time	t <sub>CKE</sub>	TBD	TBD	3		3		3		t <sub>CK</sub>	34

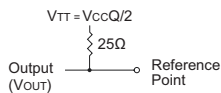
NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.



**Notes**

1. All voltages referenced to  $V_{SS}$
2. Tests for AC timing,  $I_{CC}$ , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and  $I_{CC}$  tests may use a  $V_{IL}$  to  $V_{IH}$  swing of up to 1.0V in the test environment parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between  $V_{IL}$  (AC) and  $V_{IH}$  (AC). Slew rates less than 1.0V/ns require the timing parameters to be rated as specified.
5. The AC and DC input level specifications are as defined in the SSTL\_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using  $t_{ISB}$  and the Setup and Hold Time Derating Values table.  $t_{IS}$  timing ( $t_{ISB}$ ) is referenced from  $V_{IH}$  (AC) for a rising signal and  $V_{IL}$  (AC) for a falling signal.  $t_{IH}$  timing ( $t_{IHB}$ ) is referenced from  $V_{IH}$  (AC) for a rising signal and  $V_{IL}$  (DC) for a falling signal. The timing table also lists the  $t_{ISB}$  and  $t_{IHB}$  values for a 1.0V/ns slew rate; these are the "base" values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points.  $t_{DS}$  timing ( $t_{DSB}$ ) is referenced from  $V_{IH}$  (AC) for a rising signal and  $V_{IL}$  (AC) for a falling signal.  $t_{DH}$  timing ( $t_{DHB}$ ) is referenced from  $V_{IH}$  (DC) for a rising signal and  $V_{IL}$  (DC) for a falling signal. The timing table lists the  $t_{DSB}$  and  $t_{DHB}$  values for a 1.0V/ns slew rate. If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the cross point of DQS/DQS#. Data timing is now referenced to  $V_{REF}$ , provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to  $V_{IH}$  (AC) for a rising DQS and  $V_{IL}$  (DC) for a falling DQS.
8.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (when the device output is no longer driving ( $t_{HZ}$ ) or begins driving ( $t_{LZ}$ )).
9. This maximum value is derived from the referenced test load.  $t_{HZ}$  (MAX) will prevail over  $t_{DQSCCK}$  (MAX) +  $t_{RPST}$  (MAX) condition.
10.  $t_{LZ}$  (MIN)  $t_{LZ}$  will prevail over a  $t_{DQSCCK}$  (MIN) +  $t_{RPRE}$  (MAX) condition.
11. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low or

High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above  $V_{IH}$  DC (MIN)) then it must not transition low (below  $V_{IH}$  (DC)) prior to  $t_{DQSH}$  (MIN).

12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turn around.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on  $t_{DQSS}$ .
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125μs. However, a REFRESH command must be asserted at least once every 70.3μs or  $t_{RFC}$  (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Each half-byte lane has a corresponding DQS.
16. CK and CK# input slew rate must be  $\geq 1V/ns$  ( $\geq 2V/ns$  if measured differentially).
17. The data valid window is derived by achieving other specifications -  $t_{HP}$ , ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ . For example,  $t_{CL}$  and  $t_{CH}$  are = 50 percent of the period, less the half period jitter [ $t_{JIT}(HP)$ ] of the clock source, and less the half period jitter due to cross talk [ $t_{JIT}(cross\ talk)$ ] into the clock traces.
19.  $t_{HP}$  (MIN) is the lesser of  $t_{CL}$  minimum and  $t_{CH}$  minimum actually applied to the device CK and CK# inputs.
20. READs and WRITEs with auto precharge are allowed to be issued before  $t_{RAS}$  (MIN) is satisfied since  $t_{RAS}$  lockout feature is supported in DDR2 SDRAM devices.
21.  $V_{IL}/V_{IH}$  DDR2 overshoot/undershoot. REFER to the 512Mb or 1Gb DDR2 SDRAM data sheet for more detail.
22.  $t_{DAL} = (nWR) + (t_{RP}/t_{CK})$ : For each of the terms above, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period; nWR refers to the  $t_{WR}$  parameter stored in the MR[11,10,9]. Example: For 534 at  $t_{CK} = 3.75$  ns with  $t_{WR}$  programmed to four clocks.  $t_{DAL} = 4 + (15\ ns/3.75\ ns)\ clock = 4 + (4)\ clocks = 8\ clocks$ .
23. The minimum READ to internal PRECHARGE time. This parameter is only applicable when  $t_{RTP}/2 * t_{CK} > 1$ . If  $t_{RTP}/2 * t_{CK} \leq 1$ , then equation AL + BL/2 applies. Notwithstanding,  $t_{RAS}$  (MIN) has to be satisfied as well. The DDR2 SDRAM device will automatically delay the internal PRECHARGE command until  $t_{RAS}$  (MIN) has been satisfied.
24. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
25. ODT turn-on time  $t_{AON}$  (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time  $t_{AON}$  (MAX) is when the ODT resistance is fully on. Both are measured from  $t_{AOND}$ .



26. ODT turn-off time  $t_{AOF}$  (MIN) is when the device starts to turn off ODT resistance. ODT turn off time  $t_{AOF}$  (MAX) is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .
27. This parameter has a two clock minimum requirement at any  $t_{CK}$ .
28.  $t_{DELAY}$  is calculated from  $t_{IS} + t_{CK} + t_{IH}$  so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
29.  $t_{ISXR}$  is equal to  $t_{IS}$  and is used for CKE setup time during self refresh exit.
30. No more than 4 bank ACTIVE commands may be issued in a given  $t_{FAW}$  (MIN) period.  $t_{RRRD}$  (MIN) restriction still applies. The  $t_{FAW}$  (MIN) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
31.  $t_{RPA}$  timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued,  $t_{RP}$  timing applies.  $t_{RPA}$  (MIN) applies to all 8-bank DDR2 devices.
32. Value is minimum pulse width, not the number of clock registrations.
33. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time ( $t_{WR}$ ) during auto precharge.
34.  $t_{CKE}$  (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + 2 * t_{CK} + t_{IH}$ .
35. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving ( $t_{RPST}$ ) or beginning to drive ( $t_{RPRE}$ ).
36. When DQS is used single-ended, the minimum limit is reduced by 100ps.



**ORDERING INFORMATION FOR AD6**

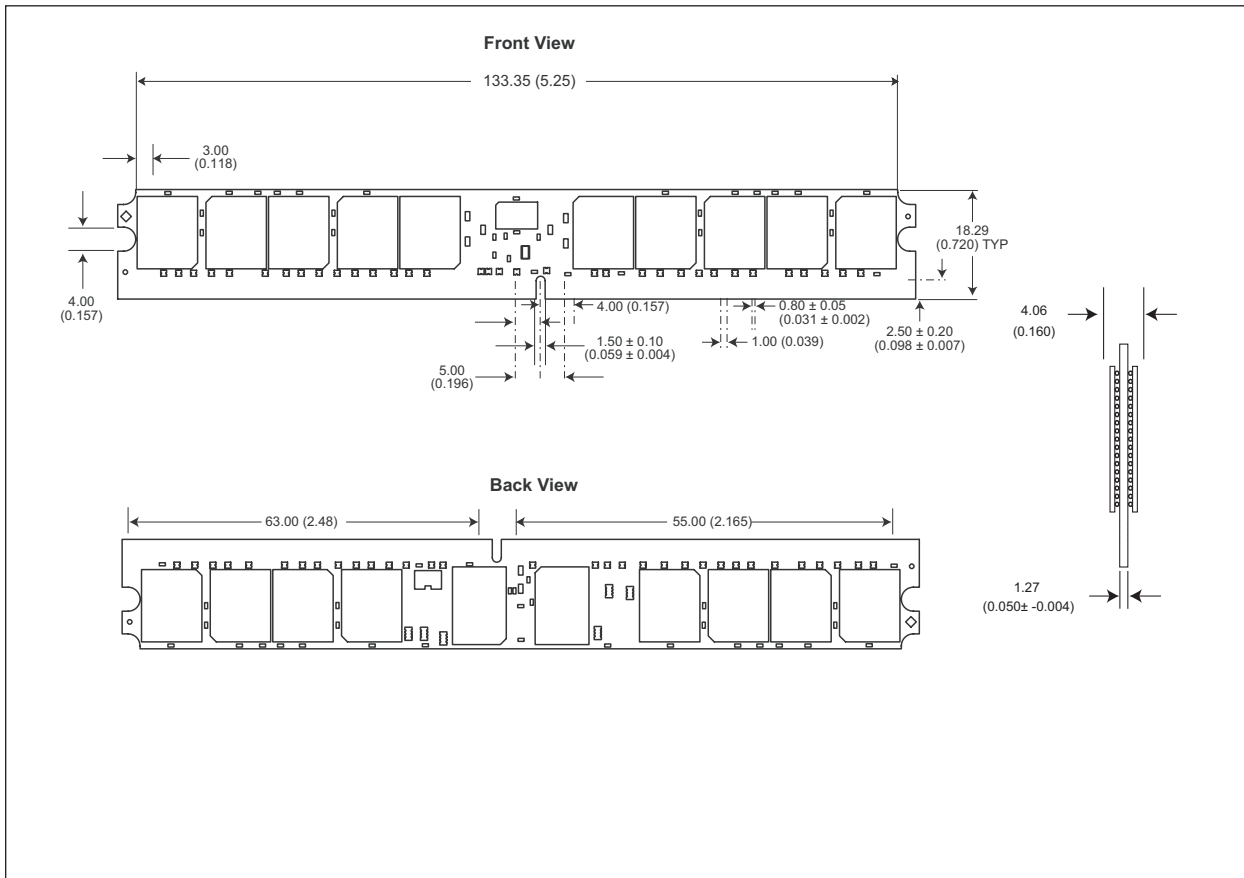
Part Number	Speed/Data Rate	CAS Latency	t <sub>RCD</sub>	t <sub>RP</sub>	Height*
W3HG2128M72ACER806AD6xG**	400MHz/800Mb/s	6	6	6	18.29mm (0.72") TYP
W3HG2128M72ACER665AD6xG**	333MHz/667Mb/s	5	5	5	18.29mm (0.72") TYP
W3HG2128M72ACER534AD6xG	266MHz/533Mb/s	4	4	4	18.29mm (0.72") TYP
W3HG2128M72ACER403AD6xG	200MHz/400Mb/s	3	3	3	18.29mm (0.72") TYP

\*\* Contact factory for availability

NOTES:

- RoHS compliant product. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

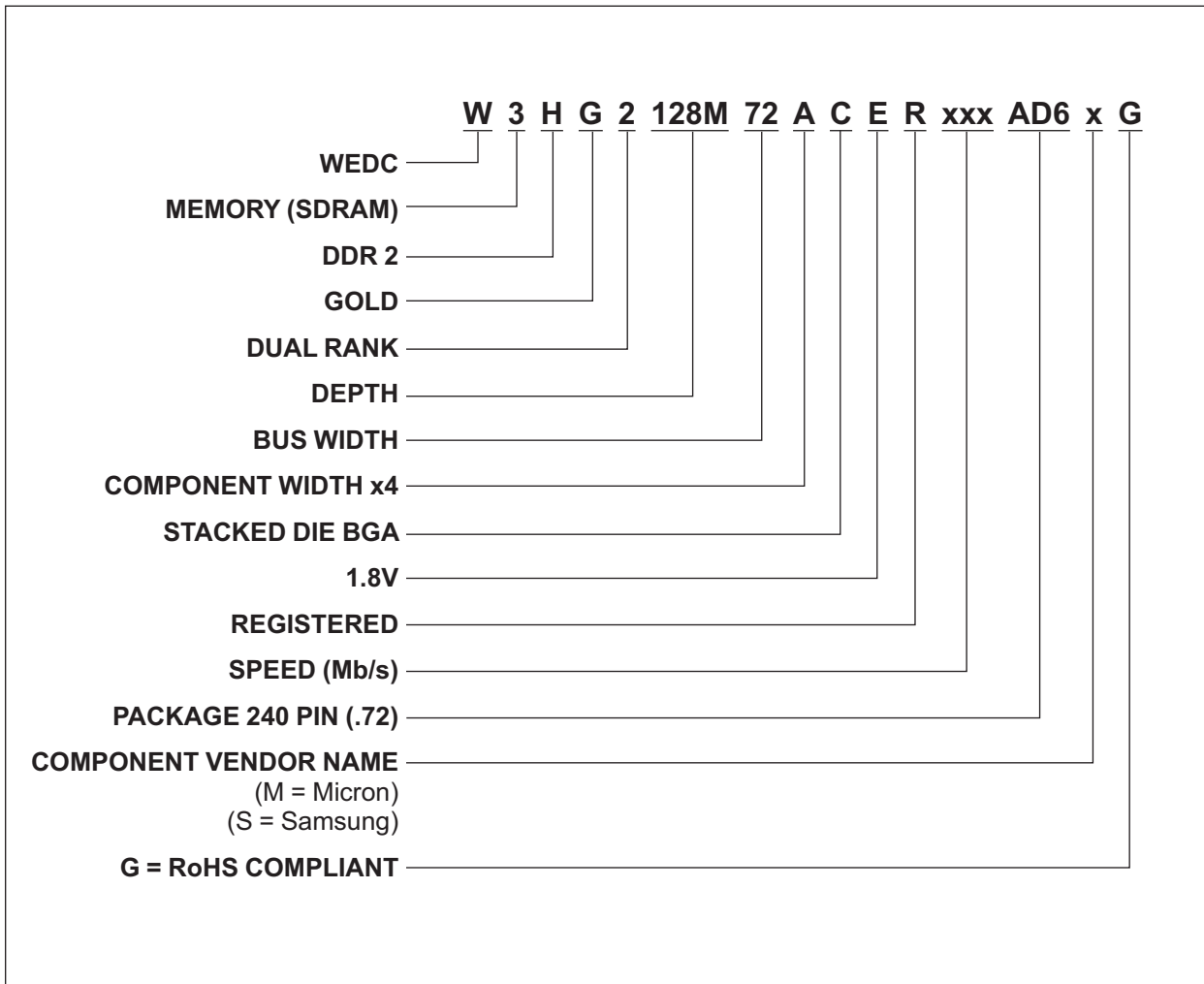
**PACKAGE DIMENSIONS FOR AD6**



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



**PART NUMBERING GUIDE**





### Document Title

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL,VLP

### Revision History

Rev #	History	Release Date	Status
Rev 0	Evaluation and review	July 2005	Concept
Rev 1	1.1 Created concept data sheet	December 2005	Concept
Rev 2	2.1 Added Icc specs 2.2 Added AC specs	December 2005	Advanced
Rev 3	3.1 Moved to Preliminary	January 2006	Preliminary
Rev 4	4.0 Updated package outline 4.1 Added "stacked die" designation "C" to part number and part number guide 4.2 Added new capacitance numbers.	February 2006	Preliminary
Rev 5	5.1 Corrected package width dimension	May 2006	Preliminary